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Closed-Loop Adaptive Frequency and Phase-Shift Control of Bidirectional Class-E^2 Converter for Energy Storage Applications

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***Abstract*— This paper presents discrete frequency and phase-shift control for a bidirectional class-E^2 converter, enabling a wide range of output power in energy storage applications. Class-E^2 converters typically operate within a narrow power range to achieve zero voltage switching (ZVS) across the switching devices and ensure high efficiency. To address this limitation, we propose an adaptive frequency control algorithm that utilizes multiple frequency steps to reduce output ripple and minimize output capacitor requirements. Our adaptive frequency control algorithm ensures high efficiency across a wide output power range by using 16 discrete switching frequency steps ranging from 800 kHz to 1.6 MHz. Duty ratios are pre-computed and stored in a lookup table to provide ZVS at each frequency. We also apply a variable phase shift between the switching devices to maintain ZVS and control the power flow direction. By directly selecting and applying the appropriate frequency from the lookup table instead of sequential searching, our proposed algorithm enables faster dynamic response with minimal undershoot and overshoot. Through simulation and implementation of closed-loop control of the bidirectional class-E^2 converter prototype using an MCU, we achieved bidirectional output power level variation from 13 W to 350 W with a maximum efficiency of 93.5%.**

***Index Terms*—Bidirectional power flow, frequency control, phase control.**

I. Introduction

Bidirectional dc-dc converters are essential in energy storage systems using lithium-ion batteries to facilitate the charging and discharging processes between the batteries, a power grid, or other electrical loads [1], [2]. To achieve high-power density in the systems, class-E^2 converters at MHz frequencies are promising solutions for minimizing size and weight. Also, their continuous currents, sinusoidal voltages across switching devices, and zero voltage switching (ZVS) operation help us to minimize electromagnetic interference (EMI) and reduce switching losses [3], [4]. However, the ZVS operation in class-E^2 converter tends to be limited to a narrow power range, especially when using infinite input/output inductors.

To overcome this issue, previous studies have proposed resistance or impedance compression network-based solutions to extend the power range [5]–[7]. However, these solutions require additional passive components, increasing the size and introducing extra losses. Also, while phase shift control has been demonstrated for controlling output power easily, its efficiency significantly decreases at lower power levels [8], [9].

In addition, continuous frequency control, typically for resonant converters such as LLC converters with switching devices at a constant 50% duty ratios, poses a challenge for class-E^2 converters because of the requirement of adjusting duty ratios across the frequency range [10]. As a result, discrete frequency control is used alone or often in conjunction with hysteretic on-off control, employing a lookup table containing frequency and corresponding duty ratio values to achieve ZVS [11]–[13]. Moreover, frequency and phase modulation is reported to remove variable frequency content with a load in [14]. These frequency and phase modulations allow us to remove low-frequency content in the output, in contrast to hysteretic frequency control or frequency control with hysteretic on/off, to simplify input/output filter design, reduce EMI, and decrease capacity fade of lithium-ion battery [15].

In all these approaches, incorporating multiple discrete frequency steps in the lookup table is necessary for achieving high efficiency over a broad power range. These multiple frequency steps provide low ripple while minimizing output capacitor size. However, a large number of steps prevents a fast dynamic response to changes in power demand in both forward and reverse power directions. Therefore, it is critical to navigate numerous discrete frequency steps to achieve high efficiency without compromising on transient response.

This paper presents closed-loop adaptive frequency and phase-shift control in a class-E^2 bidirectional dc-dc converter capable of operating within a power range of 13 W to 350 W utilizing 16 discrete frequency steps. In the forward mode, the adaptive frequency control algorithm adds an adaptive step to the lookup table index based on the error magnitude between the reference battery charge current and the measured current. This approach allows the desired frequency to be reached more quickly instead of incrementally adjusting the lookup table index for the frequency. For the reverse mode, an error between the reference voltage and the measured primary

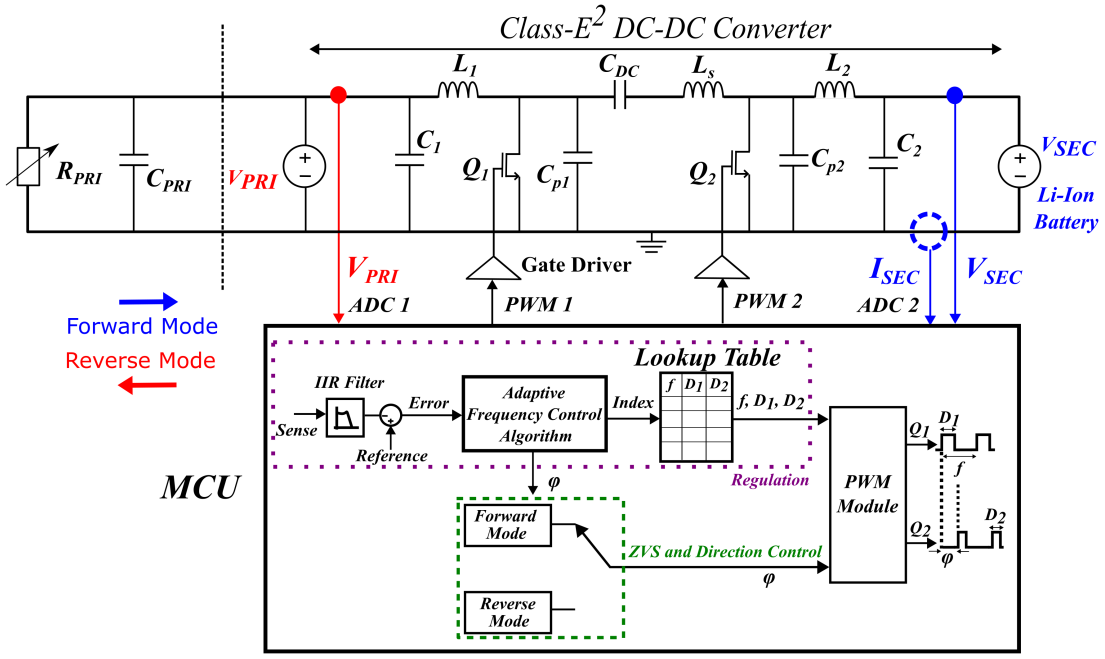


Fig. 1: Block diagram of the proposed digital closed-loop bidirectional class-E^2 dc-dc converter.

source node voltage is divided into multiple error bands, each associated with a pair of lookup table indexes corresponding to two adjacent frequencies. This approach enhances dynamic response by directly adapting to the required lookup table indexes based on the error. Additionally, the phase shift between switches is varied to achieve ZVS and change the direction of power transfer.

The remainder of the paper is structured as follows. The design methodology for the adaptive frequency and phase-shift control of bidirectional class-E^2 dc-dc converter is described in Section II. Section III presents adaptive frequency and phase-shift control simulation details, and Section IV shows the experimental results. Finally, Section V concludes the paper.

II. Adaptive Frequency and Phase-Shift Control of Bidirectional Class-E^2 Converter

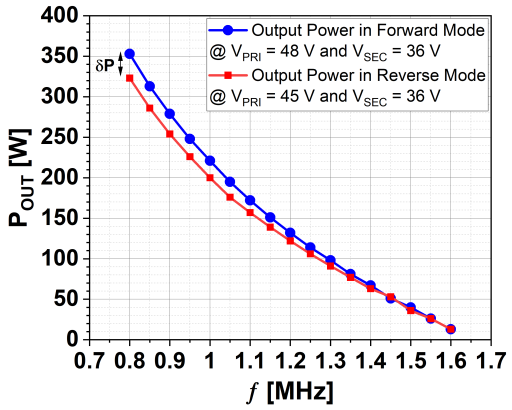
The symmetrical class-E^2 dc-dc converter with a non-resonant tank network is illustrated in Fig. 1 [14]. The primary source voltage, V_{PRI}, ranges between 48 and 50 V, while the secondary source voltage – lithium-ion battery, V_{SEC}, varies from 30 to 42 V. The non-resonant tank design of the class-E^2 dc-dc converter utilizes a large DC blocking capacitor [16]. This design approach differs from resonant tank designs that use a small capacitor in resonance with a large tank inductor. Using a non-resonant tank design, the converter power is spread across a wider frequency range compared to the equivalent resonant tank design while minimizing the size and losses associated with the series resistance of the tank inductor. With this increased frequency range, dividing the frequency into larger steps is possible.

A. Selection of Discrete Frequencies

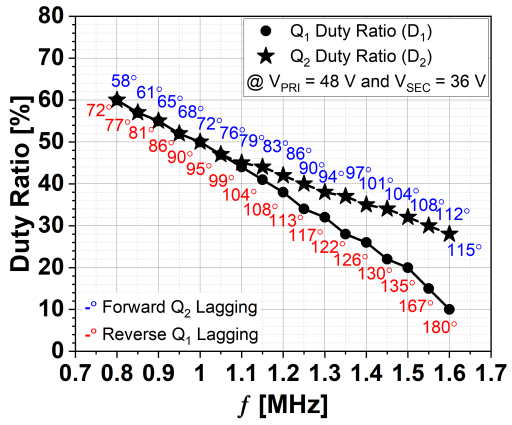
The proposed adaptive frequency and phase-shift control for the bidirectional class-E^2 converter is implemented using a microcontroller unit (MCU), as depicted in Fig. 1. The lookup table within the MCU stores the frequency and duty ratio values, and infinite impulse response (IIR) filters process all sensed quantities. The proposed adaptive frequency control algorithm also generates the required phase shift values between Q_1 and Q_2, which vary depending on the frequency and the power transfer mode.

Initially, the converter is designed with a nominal frequency of 1 MHz and switches Q_1 and Q_2 with a duty ratio of 50%. The nominal power at 1 MHz is 220 W at a nominal output of 36 V with a 48 V input. Then, the converter's minimum power requirement is set at 10 W. Based on this low power requirement, frequencies f higher than 1 MHz are then chosen in 50 kHz increments (explained in the following paragraph), and the output power P_{OUT}, duty ratios D_1 and D_2 for the converter are determined using the procedure outlined in [14]. This process is repeated until the minimum P_{OUT} is achieved, resulting in 12 frequency steps from 1 MHz to 1.6 MHz.

When determining the frequency steps, having many small steps allow for fine regulation of the battery's charge current or voltage during charging in the forward mode of power transfer. Also, when a battery is discharging in reverse mode, the output voltage of the converter is regulated by switching between two adjacent frequencies to achieve the required power. Note that this ensures that the converter provides the average power equivalent to the load demand and maintains a stable output voltage. When the adjacent frequencies are closely spaced (the frequency steps are small), it reduces the ripple in the



(a)



(b)

Fig. 2: Relationship between (a) P_{OUT} vs. frequency, and (b) Duty ratios vs. frequency at different phase shift values.

output voltage while allowing the DC-link capacitor C_{PRI} to have a smaller ripple current rating. However, the size of each frequency step is limited by the acceptable error in the regulated quantity (such as charge current), the resolution of sensors, and the MCU.

After determining the frequency steps from the nominal output power to the minimum P_{OUT} by increasing the frequency, the maximum power requirement is set at 350 W. Frequencies below 1 MHz deliver this higher power but at the cost of a reduction in converter efficiency due to increased conduction losses and thermal stress on Q_1 and Q_2. However, these brief periods of higher power than nominal power are typically encountered during battery boostcharging or constant-temperature charging [17], [18], which does not necessitate high precision in the charge current. Hence, only four frequencies lower than the nominal frequency are selected to provide higher power for a short period.

The described frequency selection procedure is carried out in the forward power transfer mode, with switch Q_2 assumed to be a diode. After determining the frequency, associated P_{OUT}, and D_1 and D_2 for Q_1 and Q_2, the phase shift ψ between Q_1 and Q_2 is ascertained using LTspice simulation to minimize losses in Q_1 and Q_2 at each frequency. The determined phase shift value is the point where the switch acting as a diode naturally conducts.

The determined relationship between power and frequency and duty ratios vs. frequency and phase shift using 16 discrete frequency steps is illustrated in Fig. 2. The lookup table includes 17 discrete frequencies with duty ratios for each. This lookup table is utilized for both forward and reverse power transfer modes, although the phase shift values vary. The first entry in the lookup table has an index of zero and corresponds to the highest frequency of 1.6 MHz with the lowest power, while the last entry has an index of 16 and corresponds to the lowest frequency of 0.8 MHz with the highest power. If necessary, additional power and duty ratios for frequencies between the 17 discrete values can be readily calculated using a polynomial curve fitting of at least a second-degree polynomial. It is important to note that while the class-E^2 converter inherently provides protection under load short-circuit conditions, it cannot operate in open-load situations. In an open-load situation, the high output voltage can immediately fail the switching devices due to high voltage stress unless the converter is protected against open-load conditions.

B. Power Transfer Mode Selection Logic

When operating the bidirectional class-E^2 dc-dc converter, the voltage measured at the input (V_{PRI}) node determines the transition between forward and reverse modes. An IIR filter is applied to the input voltage V_{PRI} to ensure accurate power transfer direction identification based solely on the input voltage to reduce high-frequency noise. This method increases the reliability of direction identification based on the V_{PRI}.

The IIR filter is designed by transforming the first-order analog filter of the form $\frac{1}{\tau s+1}$ by using backward Euler's approximation instead of the bilinear approximation for simplicity [19]:

$$y(n) = y(n-1) + \frac{T_s}{\tau}[x(n) - y(n-1)], \tag{1}$$

where τ represents the filter time constant, T_s denotes the sampling period, $x(n)$ is the sampled input value, $y(n)$ refers to the filter output at the current step, and $y(n-1)$ is the filter output at the previous step. Additionally, a hysteresis band is introduced around the voltage thresholds to prevent unintentional direction switching due to transients in V_{PRI}.

While the reverse direction voltage level at V_{PRI} node can be close to the forward voltage level of 48 V, having very close forward and reverse voltage levels causes a challenge for the control algorithm to identify the power transfer direction accurately. On the other hand, the class-E^2 functions as a constant current source, with the current magnitude determined by the operating frequency. It means that selecting a much lower voltage compared with the voltage level of 48 V is not feasible because it decreases the maximum output power provided by class-E^2 in the reverse direction. Therefore, 45 V is chosen as the voltage for regulation at V_{PRI} node in the

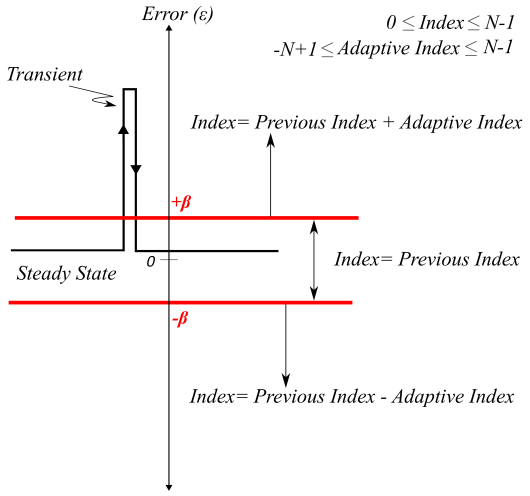


Fig. 3: Frequency index calculation for forward power transfer mode.

reverse power transfer mode to detect the power transfer direction clearly and achieve enough output power in the reverse direction. The difference in power between the forward and reverse power transfer modes is depicted by δP in Fig. 2a. This power difference is due to the selection of a lower voltage of 45 V for regulation at V_{PRI} node in the reverse power transfer mode. A 1 V hysteresis band is applied at 47 V. When the V_{PRI} node voltage falls below the hysteresis band, the Q_2 gate drive signal is configured to lead Q_1 for the reverse mode of power transfer, and when it rises above the hysteresis band, the Q_2 gate drive signal is set to lag Q_1 for forward power transfer mode.

C. Design of Adaptive Frequency and Phase-Shift Control: Forward-Mode Power Transfer

In the forward mode of power transfer, there are two main modes of operation: constant current (CC) mode, where the battery charge current I_{SEC} is maintained constant, and constant voltage (CV) mode, where the battery voltage V_{SEC} is regulated by decreasing charge current once it reaches a predetermined voltage set point.

In the CC phase of forward mode power transfer, the I_{SEC} is regulated by maintaining the error ϵ_f between the reference current and measured current (I_{SEC}) between error band $\pm\beta$:

$$\beta \geq \frac{\Delta I_{SEC}}{N} = \frac{\Delta P_{OUT}}{V_{SEC} N}, \tag{2}$$

where N is a number of discrete frequency steps, ΔI_{SEC} is the difference between maximum and minimum battery charge current, and ΔP_{OUT} is the total power range. Whenever there is a perturbation from the steady state, the index of the lookup table is changed with an adaptive index as $Index = Previous\ Index + Adaptive\ Index$ if the error is greater than β. Also, $Index = Previous\ Index - Adaptive\ Index$ if the error is less than $-\beta$. The index increment/decrement rate δT is determined based on the time that the converter takes to reach a steady state every time the index changes. The value of the adaptive index is determined based on the magnitude of the error ϵ_f, and β as:

$$Adaptive\ Index = \begin{cases} round\left[\frac{1}{\beta}(\epsilon_f - \beta)\right], & if\ \epsilon_f > \beta, \\ round\left[-\frac{1}{\beta}(\epsilon_f + \beta)\right], & if\ \epsilon_f < -\beta. \\ 0, & \text{otherwise.} \end{cases} \tag{3}$$

This equation determines how many lookup table indexes should be incremented or decremented to bring the error back within the error band $\pm\beta$, as represented in Fig. 3. For example, when the error exceeds β, the adaptive index is calculated as $\frac{1}{\beta}(\epsilon_f - \beta)$ with the round function to ensure that the adaptive index is an integer value. We also include the case when the error is less than $-\beta$ to account for the case when the measured current is above the reference current. By adaptively adjusting the lookup table index based on the error magnitude, the algorithm rapidly converges to the desired current value instead of sequentially incrementing or decrementing the lookup table index. The chosen rate for index updation δT must be higher than the time the converter takes to reach a steady state every time the index (frequency) changes to reduce total harmonic distortion in the output of the converter.

In the CV mode, when V_{SEC} meets or exceeds a predetermined set battery voltage point, the index is decremented (frequency is incremented) to reduce charge current at a predefined interval, δT. This decrement continues from the last operating index in the CC mode to the index of zero sequentially to regulate V_{SEC} by decreasing the I_{SEC}. The utilization of larger discrete frequency steps by the proposed algorithm mimics the CV mode characteristics seen in other converter topologies, such as LLC [20]. This approach reduces the battery charging time in CV mode since the current always decrements by a small amount.

D. Design of Adaptive Frequency and Phase-Shift Control: Reverse-Mode Power Transfer

In the reverse mode of power transfer, the primary focus is on regulating V_{PRI} node against variation in R_{PRI}. Importantly, the primary objective driving control in the reverse mode is to minimize ripple, undershoot/overshoot, and settling time at V_{PRI} node while reducing the size of the DC-link capacitor C_{PRI}. Therefore, unlike the forward-mode transfer where I_{SEC} is allowed to go outside the error band during transients, we restrict the error ϵ_r between a reference voltage and V_{PRI} node voltage within $\pm\alpha$ at all times for index computation where α:

$$\alpha \geq \frac{1}{2C_{PRI}} \frac{V_{PRI}}{R_{PRI(min)}} \delta T. \tag{4}$$

To maintain error within an error band of $\pm\alpha$, the error between the reference voltage and measured voltage at V_{PRI}

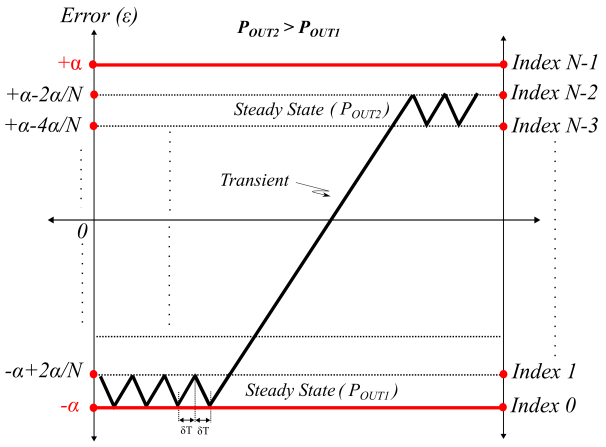


Fig. 4: Assignment of frequency indices across multiple error bands for reverse power transfer mode.

node is divided into multiple smaller error bands of $2\alpha/N$, each assigned to different indexes:

$$Index = round\left[\frac{N-1}{2\alpha}(\epsilon_r + \alpha)\right], \tag{5}$$

where 2α represents the width of the total error.

Whenever a transient occurs because of a change in output power requirement P_{OUT}, such as from P_{OUT1} to P_{OUT2} or vice versa, the error increases or decreases. To regulate V_{PRI} node against P_{OUT} variations, the frequency index automatically adapts between two adjacent frequencies based on the error to provide the required P_{OUT} as illustrated in Fig. 4.

As the number of frequency steps increases, the number of necessary error bands also grows, causing the error to be distributed over a broader range ($\pm\alpha$), deviating from zero error. Consequently, it is crucial to minimize the width of each error band to reduce the steady-state error. This minimum width of an error band is influenced by the equivalent series resistance (ESR) and equivalent series inductance (ESL) of the C_{PRI}, the resolution of the voltage sensor, and the analog-to-digital converter (ADC).

III. Simulation Analysis

As discussed earlier, to determine the optimal phase shifts for achieving ZVS at each frequency across both forward and reverse power transfer modes, we conducted LTspice simulations of the class-E^2 converter. We employed the component values specified in Table I and utilized f, D_1, and D_2 from Section II-A. The GS66508B eGaN transistor spice model [21] was also incorporated in the simulation. As illustrated in Fig. 5, we selected the optimal phase shift values that yielded the highest efficiency and minimal power losses in the switches, Q_1 and Q_2. This approach is repeated to determine the optimal phase shift at every other frequency. In order to achieve ZVS and control the direction of power

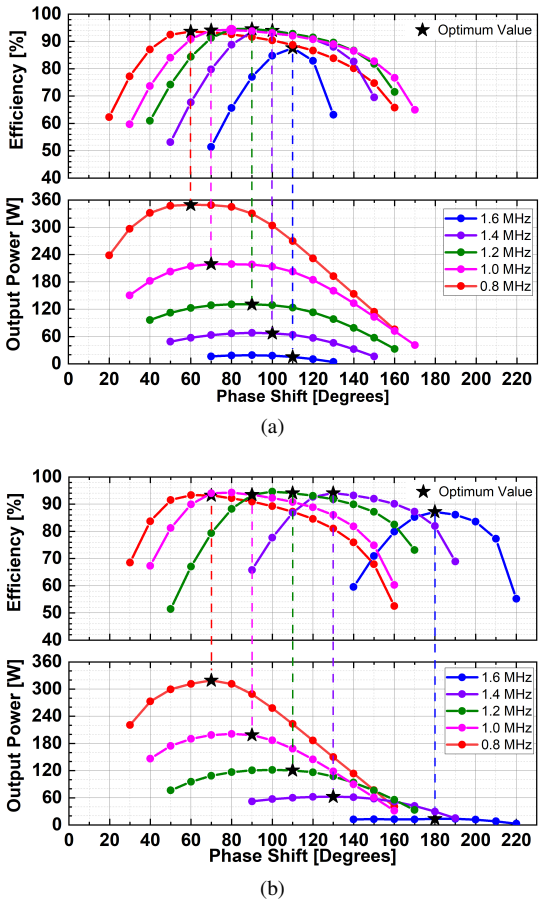
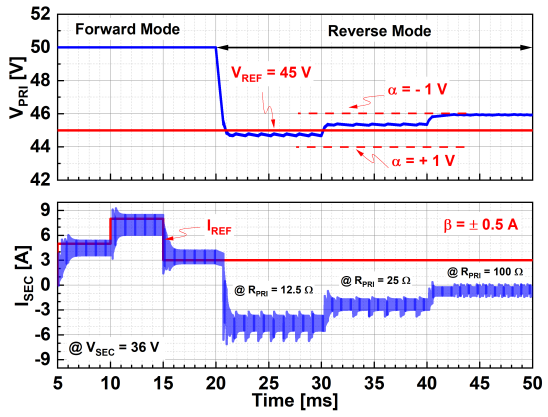


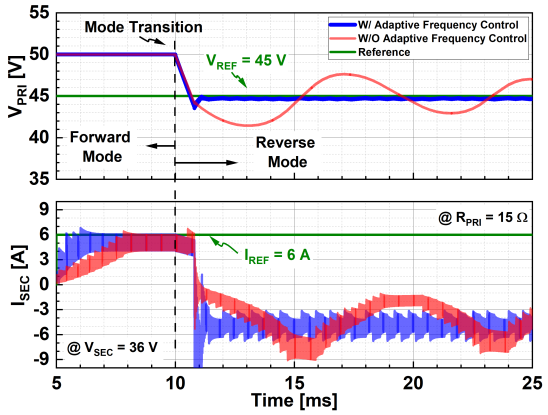
Fig. 5: LTspice simulation results illustrating optimal phase-shift determination between Q_1 and Q_2: (a) In a forward mode, where Q_2 is lagging, and (b) In a reverse mode, where Q_1 is lagging.

transfer, Q_2 lagged Q_1 in the forward power transfer mode, while Q_1 lagged Q_2 in the reverse power transfer mode. It is important to note that the degree of phase shift at a specific frequency varied based on the power transfer mode, as illustrated in Fig. 5a and Fig. 5b. Once the phase shift values were determined, the corresponding time delay between Q_1 and Q_2 were calculated using the frequency value.

Using the frequency, duty ratios, and phase shift values obtained from LTspice, we simulated the bidirectional class-E^2 converter in PLECS. The PLECS simulation utilized a C-coder for closed-loop control [22]. The analog filters for charge current I_{SEC}, with a cut-off frequency of 1 kHz, and for voltage V_{PRI}, with a cut-off frequency of 16 kHz, were converted into digital filters using the backward Euler transformation, as described in (1). For the simulation, we assumed the ESR of capacitor C_{PRI} to be 20 $m\Omega$ and neglected its ESL, assuming it is small, to focus on the primary dynamics of the converter. However, the capacitor with high values of ESR and ESL increases the output ripple and, therefore, the value of α for error band distribution in reverse power transfer mode. The parameters α and β were



(a)



(b)

Fig. 6: PLECS simulation results: (a) Transient response to step changes, and (b) Comparison between scenarios with and without adaptive frequency control.

set at 1 V and 0.5 A, respectively. The simulation used a sampling frequency of 50 kHz for I_{SEC}, V_{SEC}, and V_{PRI} and an interval δT of 300 μs was used based on the time required for the converter to reach a steady state.

As depicted in Fig. 6a, during the forward power transfer mode, the V_{PRI} was set at 50 V and V_{SEC} to 36 V. The battery charged at a constant current of 5 A, with a step change to 8 A occurring at 10 ms and a subsequent step change to 3 A at 15 ms, all the while maintaining an error within $\pm$ β. When power generation at V_{PRI} is lost at 20 ms, the input node voltage to the class-E^2 dc-dc converter starts to decrease, with power flow reversal taking place within approximately 1 ms. In reverse power transfer mode, the class-E^2 dc-dc converter regulated the input node V_{PRI} to remain within 45 V $\pm$ α. Even when load R_{PRI} was varied between 12.5 Ω to 100 Ω, the V_{PRI} node voltage settled within 45 V $\pm$ α without any overshoot. In every transient scenario described above, the minimum losses in switches Q_1 and Q_2 were maintained through ZVS, achieved by using pre-calculated frequency, duty ratios, and phase shift between Q_1 and Q_2.

We also compared frequency and phase-shift control – with

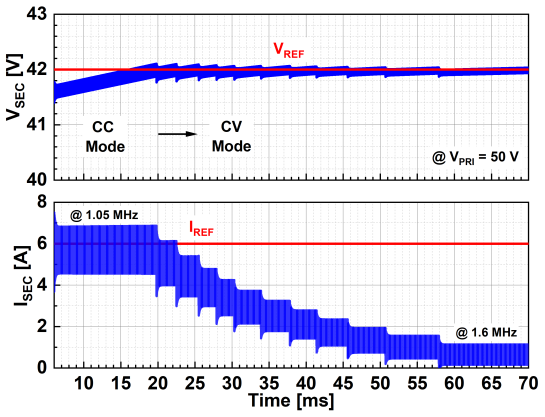


Fig. 7: PLECS simulation results showing the performance in CV mode.

and without adaptive frequency control, as shown in Fig. 6b. Without adaptive frequency control, the index was incremented or decremented by one only when the error exceeded the single error band of $\pm$ 0.5 A for I_{SEC} in the forward mode and $\pm$ 1 V for V_{PRI} in the reverse mode. The results highlight the enhanced transient response provided by the proposed adaptive frequency and phase-shift control algorithm, especially for voltage at V_{PRI} node of 45 V in reverse mode, with nearly zero voltage undershoot and settling time of 1 ms.

To simulate the CV mode, as shown in Fig. 7, we used a simplified battery model with a capacitance of 200 mF and ESR of 0.1 Ω. A battery voltage reference of 42 V was set. When the battery voltage reaches this set voltage, the index is decremented, which in turn increases the frequency in small steps. This gradual adjustment of frequency enables the battery to charge up to its full voltage of 42 V by reducing the charge current.

IV. Experimental Results

As shown in Fig. 8, we built a prototype of a bidirectional class-E^2 converter. A heatsink from Advanced Thermal

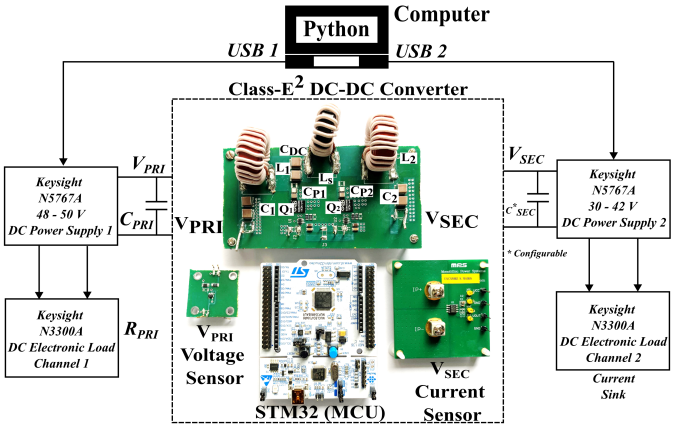


Fig. 8: Test setup for bidirectional power transfer.

TABLE I: Components specification of the class-E^2 bidirectional converter.

Parameter	Value	Type
R_{PRI}	7.5 Ω−100 Ω	N3300A DC electronic load (Keysight)
C_{PRI}	1000 μF	Aluminum Electrolytic (Low ESR)
C_1, C_2	1.32 μF	Ceramic C0G (NP0) 0.33 μF × 4
L_1, L_2	10 μH	Powdered iron core (10 µ) T106-2 (MICROMETALS) 660 × 46 AWG Litz wire 27 Turns
C_{P1}, C_{P2}	11.8 nF	Ceramic C0G (NP0)
L_s	1.6 μH	Powdered iron core (6 µ) T94-10 (MICROMETALS) 924 × 46 AWG Litz wire 16 Turns
C_{DC}	1.32 μF	Ceramic C0G (NP0)
Q_1, Q_2	GS66508B	eGaN Transistor (GaN Systems)
Gate Driver	LM5114B	Texas Instruments

Solutions, along with a thermal pad for the interface from 3M and forced-air cooling, was employed to handle the heat dissipation in Q_1 and Q_2. For the implementation of the adaptive frequency control algorithm, low-pass IIR filters, and mode transition logic, we used a low-cost Nucleo−64 board that houses an STM32F334R8T6 MCU from STMicroelectronics. This MCU's High-Resolution Timer (HRTIM) with a maximum resolution of 217 ps was set for Pulse Width Modulation (PWM). The frequency and duty ratios for the switching devices, Q_1 and Q_2, were stored in a lookup table. For forward direction regulation of I_{SEC}, a bidirectional MCS1800 current sensor evaluation board was employed, while for the regulation of V_{PRI} node in the reverse mode of power transfer, we used a voltage sensor composed of resistor dividers with 100 kΩ and 6.04 kΩ chip resistors. The 12-bit ADC was configured to sample at a frequency of 50 kHz.

We carried out a bidirectional operation test of the class-E^2 dc-dc converter using the test setup illustrated in Fig. 8. In this test setup, Channel 1 of the electronic load functioned as R_{PRI}, while Channel 2 of the electronic load was connected across power supply 2 to serve as a current sink. We wrote a Python script to control the on/off states of the power supplies for bidirectional power transfer testing.

The results of the experiment, recorded on the oscilloscope, are shown in Fig. 9. As shown in Fig. 9, we maintained a regulated I_{SEC} at 3 A during the forward mode, while V_{PRI} node was regulated roughly to 45 V in the reverse mode. Power flow direction control was achieved by generating time delays where Q_1 leads Q_2 in the forward mode and Q_1 lags Q_2 in the reverse mode. Given that the frequency is not constant, the phase shift between Q_1 and Q_2 also changes, which was true in both forward and reverse power transfer modes.

In the reverse power transfer mode, load transients were

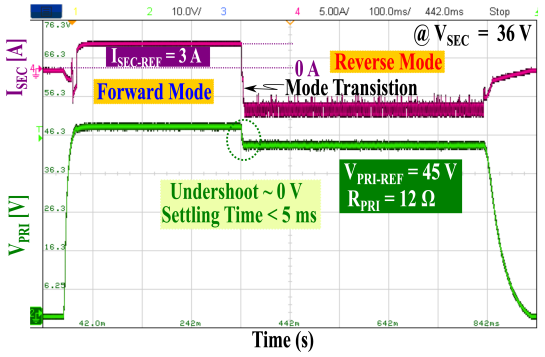
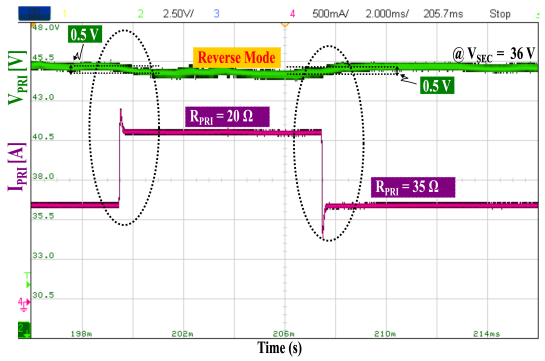
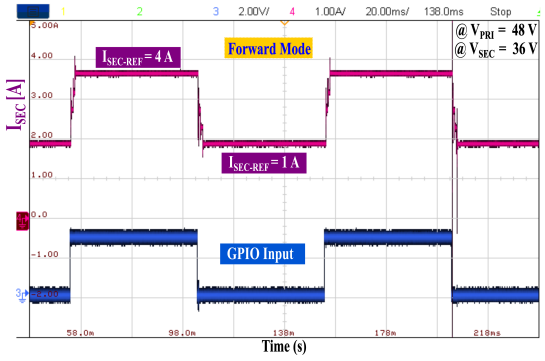


Fig. 9: Experimental results showing bidirectional power flow with adaptive frequency and phase-shift control.

carried out at V_{PRI} node from R_{PRI} of 20 Ω to 35 Ω, as shown in Fig. 10a. The voltage at V_{PRI} node is regulated within ± 1 V from a voltage reference of 45 V. Also, Fig. 10b illustrates that in the forward mode of power transfer, I_{SEC} tracked step change in the reference current carried out via General Purpose Input/Output (GPIO) input. The use of pre-computed frequency, duty ratio, and phase shift maintain ZVS during transient conditions. Our developed adaptive frequency



(a)



(b)

Fig. 10: Dynamic response: (a) Measured V_{PRI} node voltage and I_{PRI} for transient response to step changes in R_{PRI}, and (b) Measured step change in I_{SEC} in response to $I_{SEC-REF}$ variation via GPIO input.

and phase-shift control algorithm successfully attained ZVS and operated bi-directionally with a maximum efficiency of 93.5% at a power level of 216 W with an input voltage of 48 V and output voltage of 36 V. In the reverse mode of power transfer, a maximum efficiency of 92.1% was obtained at a power level of 196 W with an input voltage of 36 V and output voltage of 45 V.

V. Conclusion

This paper presents closed-loop adaptive frequency and phase-shift control of a bidirectional class-E^2 converter to provide high efficiency while achieving a fast transient response. An adaptive frequency and phase-shift control algorithm with 16 discrete frequency steps was demonstrated for enhanced dynamic response and maximum power efficiency of 93.5%. The proposed control algorithm regulated battery charge current, battery voltage in the forward power transfer mode, and input primary source voltage node in the reverse power transfer mode for the class-E^2 converter. The closed-loop performance of the converter was simulated and compared with a prototype of the class-E^2 converter using an STM32 MCU. The settling time of the converter was less than 5 ms without any undershoot/overshoot.

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