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Simulation of Low Power SDR on an FPGA for Intersatellite Communication Using MATLAB and Simulink

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“Simulation of Low Power SDR on an FPGA For Inter-satellite Communication Using MATLAB and Simulink”

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Abstract— The explosive increase within the ways and approach by using which human beings want to speak – statistics verbal exchange structures, speech communications, video communications, telecast messaging, control and command communications, disaster response communications, and soon. It is grow to be enterprise important in an effort to alter radio gadgets hastily and cost-correctly. SDR generation gives community operators and product builders the versatility, cost efficiency, and strength they need to move communications ahead, with the far benefits for stop users. SDR is a radio has a few or all of its middle network functions defined by means of software program. SDR is a radio-frequency wi-fi verbal exchange tool that may be modified the usage of software, described via software program. A software-defined radio is something that has some or all of its physical layer operations distinctive by software.

Keywords— SDR, FPGA, synchronization, low-density parity check code, intersatellite communication.

I. INTRODUCTION

In recent years, small spacecraft have piqued attention as a means of launching research missions into or beyond lower earth orbit. Because of their low value, portable, quick lead time, and small length, small satellites are becoming an increasingly significant aspect of small spacecraft missions. Hundreds of small satellites flying in formation can perform more missions, such as higher accuracy navigation, formation control, data interchange, information processing, and spacecraft maintenance. To merge the processing power, software, and hardware, all of the satellites must communicate with one another in order to remain operational. ISC’s with real time processing plays crucial for a huge number of tiny satellite to function as a community. A communication system with real-time transmission, high data throughput, and a low bit error rate is needed for an effective ISC. In most instances, the open system interconnection and by-product fashions are used to outline the shape of ISCs. The OSI physical layer's primary factors include platform, code system, & frequency allocation. The choice of a frequency range for ISCs is constrained spectrum allotted by International Telecommunication Union, the hardware that is available, the energy source, the antenna length, and the challenge requirements. S-, k-, and okay a-bands are frequently considered as options for frequency allotment for ISC. It is also believed that a higher ISC frequency makes a larger bandwidth available in addition to assisting in reducing the weight and size of the transceivers antennas.

SDRs could be very advantageous for cellular services, which must handle numerous radio protocols that are continually changing in real time. Today, the foundational radio modem technologies can be built using software-defined radio. SDR technology is anticipated to take over radio communications in the long term. In the optimal scenario, it is advised to use offset-QPSK and binary-PSK for intersatellite communication. Coherent BPSK systems have increased sensitivity for tracking and communication while using less power at the same are preferred in the Inter Satellite Communication. A Coherent Binary Phase Shift Keying systems have increased sensitivity for tracking and communication while using less power at the same level of bit error rate. By including two bits of information in each symbol, QPSK can increase spectral efficiency. Offset QPSK also solves the abrupt phase change issue in Quadrature Phase Shift Keying, Bit Error Rate level by y carrying 2-bit information in each symbol, Quadrature Phase Shift Keying can increase spectral efficiency, and Offset QPSK gets around QPSK's issue with abrupt phase changes.

II. PROPOSED SOLUTION

To overcome these barriers, real-time intersatellite communications (ISCs) are needed and to make a huge number of tiny satellites function as a n/w. This is possible with the aid of a dependable and adaptable communication infrastructure. Real-time transmission, a fast data throughput, and a low bit error rate (BER) are necessary for an efficient ISC. Both a system design for ISCs and an entire SDR concept are suggested. The proposed SDR employs better LDPC channel coding and QPSK modulation techniques. The designs of the respective Transmitter and Receiver models are displayed below.

III. DESIGN

To overcome the challenges like low data rate, more bit error rate, lower efficient, higher cost and system with no reliable and flexible, we are using the simple SDR concept. SDR is a communication system which uses software for the modulation and demodulation of radio signal. software defined radio is defined as a radio in which few or all its physical-layers operates as software defined. SDR technology brings higher data rate, low bit error rate, higher efficient, lower cost, low power and system with reliable and flexible. This implementation's task is to bring the radio that is able to communicate & receive radio protocols usually by utilizing updated software.

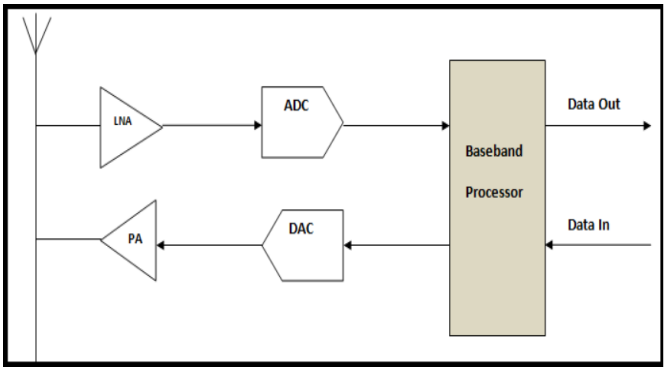

Fig. 1. Simple Block Diagram of a SDR system

The input data or signal is provided to the baseband processor that produces the baseband preprocessing signal. The baseband preprocessing signal is passed to the digital-to-analog converter and sent to the channel. In receiver, the data is received through channel and sent to the ADC converter for original signal. The original signal is received by the digital processor.

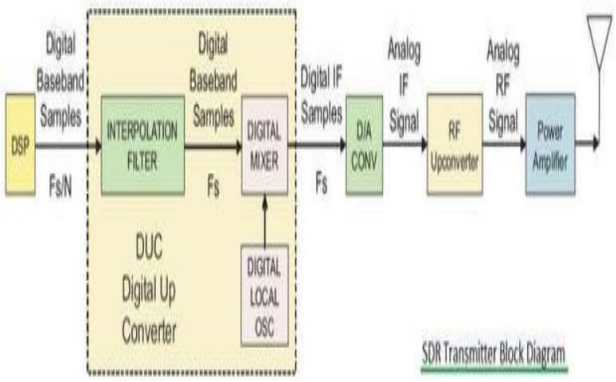

Fig. 2. SDR Transmitter Architecture

This figure.2 shows the transmitter architecture of the Software Defined Radio. As shown, it includes Digital Signal Processor(DSP), Digital-Up-Converter (DUC), Digital to Analog Conversion (D/A Conv), Analog Radio Frequency(RF) Up converter, finally Power Amplifier. Digital Up and Digital-Down-Converters normally for signal rates in communication systems. Digital up converter is employed for the conversion of the signal to intermediate frequency (IF) band from the baseband signal.
In addition to sample rate conversion, Digital-Up-Converter (DUC) and Digital-Down-Converter (DDCs) involves frequency shifts employing a mixer circuit.
With DUC (Digital Up-Conversion) it is up-converted digitally using a Digital Local Oscillator (LO) and a mixer. Analog IF signals are created from digital IF sample data. An RF up converter is used to convert this analog IF (intermediate frequency) to analogue RF (radio frequency). Before being broadcast into the air, the RF signal is amplified using the proper antenna for the intended system operating frequency.

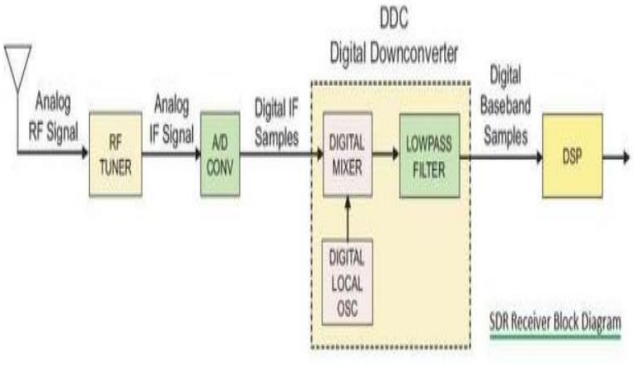

Fig.3 SDR Receiver Architecture

RF tuner is the initial module. The HF signal is changed by this HF tuner into an amplified IF signal. substitutes for the first three modules (HF amplifier, mixer, IF amplifier). A/D converter: Transforms digital IF samples into analogue IF samples. Digital down conversion, also known as DDC, transforms digital samples into digital baseband samples from digital IF samples. A low-pass FIR filter, a digital local oscillator (LO), and a digital mixer make up the DDC. To perform activities like demodulation, encoding, and other requirements as needed, algorithms are translated to a DSP processor, which receives digital baseband samples. SDR, or software defined radio, is the name of this digital implementation-based architecture.

IV.IMPLEMENTATION

For the purpose of coping with static frequency offsets, temporal shifts, and Gaussian noise, this sample model performs all the necessary work in a complicated baseband. This example is a real-world digital that addresses the aforementioned problems by using Phase Locked Loop based frame synchronisation & symbol timing recovery, fine Phase Locked Loop based freq.compensation, phase ambiguity resolution and Phase Locked Loop based coarse correlation-based compensation.

TRANSMITTER

Bit Generator: Creates data bits for frame.
a QPSK Modulator produces QPSK symbols from input data.
Two QPSK symbols are up-sampled using **a raised cosine transmission.**
A transmitter has bit generating system, The bit generating sub-system's frame payload is represented by the MATLAB workspace variable, as seen in the illustration below. There are 20 headers and "Hello world ###" messages in each frame. Two 13-bit barker codes are used to oversample the header bits, which make up the first 26 bits. For eventual usage in the receiver model's data decoding subsystem, A total of 13 QPSK symbols are produced by oversampling the barker code twice. User data fills in the remaining bits. "Hello World ###" is encoded as the payload's ASCII equivalent. A series of "000," "001," "002,"..., "099" are repeated to form the word "###" in this case. For the receiver model's clock recovery operation, To ensure an even distribution of 0s and 1s, the payload is scrambled. It uses a QPSK modulator to modulate the encrypted bits. Two raised cosine transmission filters with a roll-off factor of 0.5 are used to up sample the modulated symbol. 100,000 samples per second are sampled after the increased cosine transmission filter, which has a symbol rate of 50,000 symbols per second.

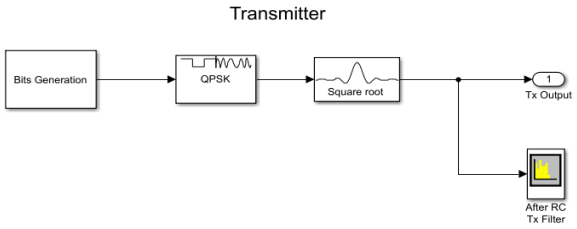

Fig. 3 SDR Transmitter Model

CHANNEL

Timing drift & Frequency offset along with WGN (White Gaussian Noise) applied for a signal using the AWGN Offset channel with customizable frequency time delay.
The transmit signal is initially subjected to the frequency offset and predetermined phase offset with variable delay frequency offset of an AWGN channel. Then, select one of the two delay types shown below to add a variable delay to your signal:

Ramp Delay: This delay type advances linearly at the rate of the Delay Step sample for each frame after being initialised with the Delay Start sample. The delay buffer fills up when the real delay reaches one frame, keeping the delay at one frame.

Triangle delay – This delay type linearly alternates B/W Minimum Delay and Maximum Delay are samples at the rate of the sample on a frame-by-frame basis.

RECEIVER

Raised cosine receive filter - Utilizes 0.5 roll-off factor.

The coarse frequency compensation method determines and corrects the signal's approximate frequency offset. At the best possible sampling time, the decision is taken.

Resampling the input signal in accordance with the recovered clock signal by using symbol-synchronizer ensures that symbol is determined at the ideal sampling time.

Preamble Detector: Recognizes Frame Header Position Frame Synchronizer: Aligns Frame Boundary to Known Frame Header

By Carrier Data Demodulation synchronizer-induced phase ambiguity is corrected, the signal is demodulated, and the text message is decoded.

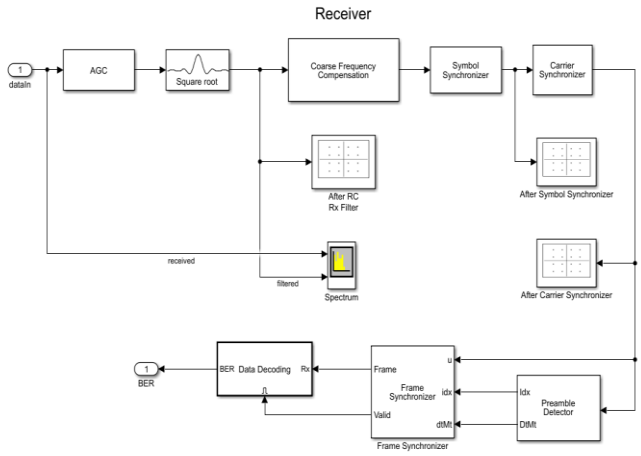

Fig. 5. SDR Receiver Model

Receive Filter with Raised Cosine

The broadcast waveform is matched with a 0.5 roll-off factor by the raised cosine receive filter.

AGC

The precision using carrier-synchronizer & symbol-synchronizer is influenced by received signal using amplitude. Achieve the best loop design, it is required to stabilise the signal amplitude. The output power AGC level that ensures the proper gain of the timing error and phase detectors are consistent across time. By using an oversampling factor of 2, the amplitude of the signal can be observed, increasing the estimation's accuracy, because the AGC is positioned in front increased cosine-receive filter.

Coarse Frequency Compensation

The subsystem for coarse frequency adjustment that verifies the user signal using estimate of the freq.off-set. A subsystem whose estimated frequency offset is depicted in the accompanying picture was created by averaging the results of the coarse frequency compensator block's correlation-based method. The phase/frequency offset block offers compensation. The constellation often spins slowly, leaving freq.offset after the frequency correction. This residual frequency is adjusted by the carrier synchronizer block.

Symbol Synchronizer

Symbol Synchronizer Library block executes clock recovery to fix timing issues in the received signal. With the Gardner algorithm, which is rotation-invariant, the timing error detector is estimated. In other words, you can apply this algorithm either before or after frequency offset correction. There are two oversampled inputs into the block. For every two input samples. There are additional symbols of o|p frame, though, when channel timing error (delay) is close to the symbol limit. A variable size signal is produced by this block since it employs bit stuffing and skip in this instance.

Adjustable block parameters include "Detector Gain," "Detector Gain", and "Normalized Loop Bandwidth." The PLL locks timing quickly and makes timing corrections with minimum timing jitter since the default values are 1.

Carrier Synchronizer

A Carrier Synchronizer library block carries out fine frequency adjustment and monitors the remaining phase offset and frequency offset of the input signal. For the purpose of correcting for residual frequency and phase shift, the PLL employs a direct digital synthesiser (DDS). The output of the loop filter's phase error integral is the DDS phase offset estimate.

The crucial damping value is set by default for one and default value for each parameter is set to 0.01, correspondingly, allowing the PLL to lock rapidly.

Preamble Detector & Frame Synchronizer

Preamble Detector Library block finds known frame header positions, and the MATLAB system block uses the Frame Synchronizer System TM object to synchronise frames. The QPSK modulation barker code is used by the preamble detector block to correlate with the received QPSK symbol and identify the position of the frame header. This positional data is used by the frame synchronizer block. Additionally, the changes it Symbol Synchronizer block's variable size output into the fixed size frames required for further processing the block's second o|p which determines whether legitimate appropriate &if it is launches subsystem.

Data Decoding

This is a capable subsystem carries out text message decoding, demodulation, and phase disambiguation. A phase may become unclear as a result. This phase shift is determined by the subsystem for phase off-set estimate is rotated with the predicted by which then demodulates the corrected data. Time the simulation is finished, payload bits have been decrypted and output to the Simulink Diagnostic Viewer.

V. RESULTS AND DISPLAYS

By running the simulation, you will see the bit error rate and a large number of graphic results.

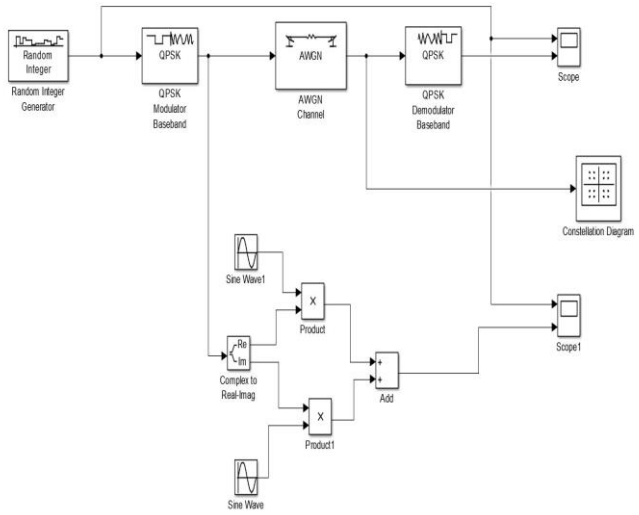

Fig6. SDR Working Model

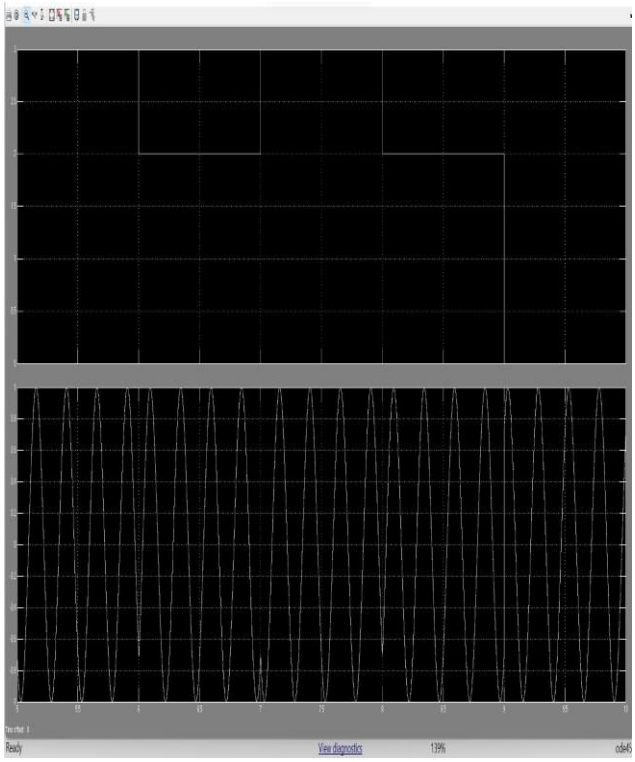

Fig7. Waveform at QPSK Modulator

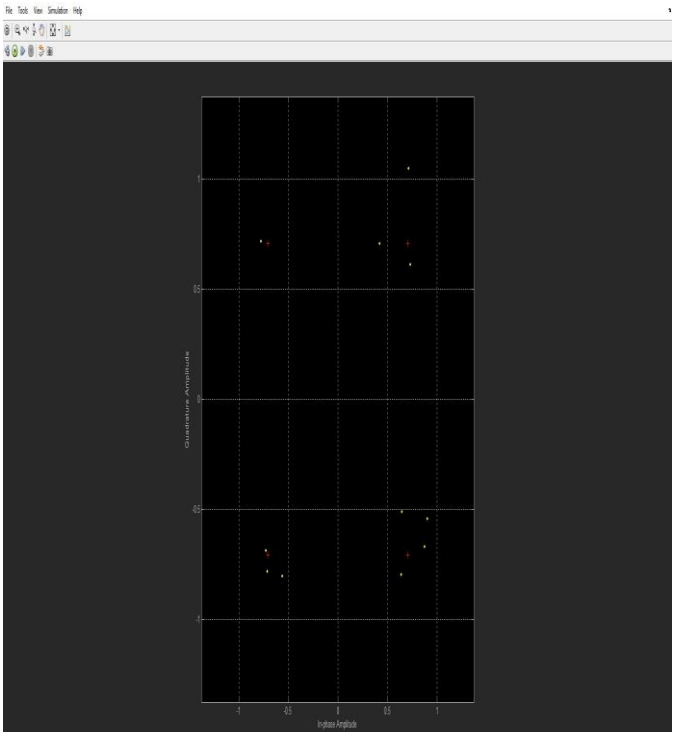

Fig8. Constellation Diagram after the AWGN Channel

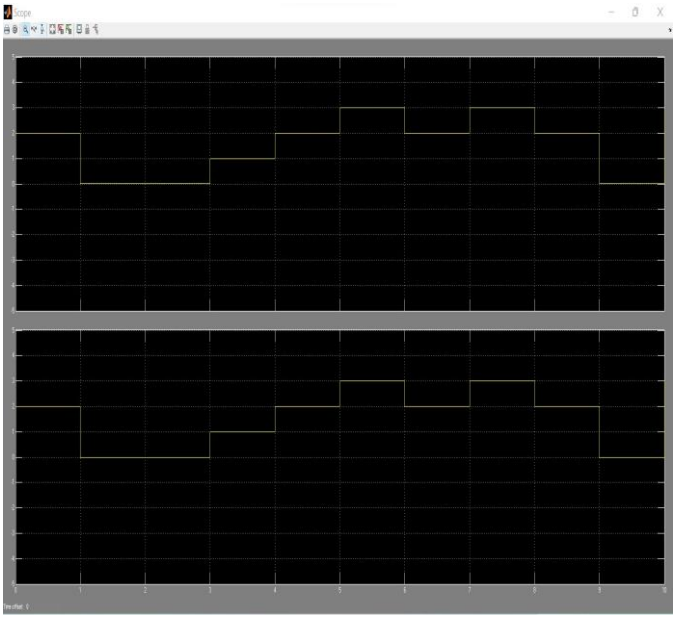

Fig9. Input waveform and Output Waveforms at QPSK Demodulator

VI. CONCLUSION

An SDR for low frequency transmitter-receiver was successfully developed. The measured findings demonstrate that the transmitter input and receiver output are identical. Furthermore, it offers a low-cost, low-power option. The architecture may be successfully reconfigurable through the use of FPGA implementation's additional flexibility in adapting to various modulation techniques, data rates, carrier frequencies, and filter types. Instead of throwing out outdated hardware's, whenever the requirements specifications change. This saves time and money. Additionally growing in popularity is the SDR platform. The suggested SDR is ready to use and appropriate for the power-constrained tiny satellite system. The frequency correction, decoder, and AGC modules have all been optimised to use fewer hardware resources. Based on the modified MSA, a condensed decoder for the is created. Performance is somewhat decreased and hardware consumption is reduced by two-thirds as a result of the simplification. Additionally, the transmitter and receiver successfully demonstrate wireless transmission when used with an FPGA-based SDR platform.

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